ABSTRACT OF THE DISCLOSURE

The present invention describes a method for creating a differential polish rate across a semiconductor wafer . The profile or topography of the semiconductor wafer is determined by locating the high points and low points of the wafer profile. The groove pattern of a polish pad is then adjusted to optimize the polish rate with respect to the particular wafer profile. By increasing the groove depth, width, and/or density of the groove pattern of the polish pad the polish rate may be increased in the areas that correspond to the high points of the wafer profile. By decreasing the groove depth, width, and/or density of the groove pattern of the polish pad the polish rate may be decreased in the areas that correspond to the low points of the wafer profile. A combination of these effects may be desirable in order to stabilize the polish rate across the wafer surface in order to improve the planarization of the polishing process.